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REVIEW

Characterization and Digital Signal Integrity Analysis of pHEMT Using an Eye Diagram

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Abstract:

Digital Performance analysis of high electron devices used in microwave communication systems is crucial for ensuring their suitability to ever-increasing high-speed data rate applications. This study aims at characterizing a 0.5x200μm dimension pseudomorphic heterojunction transistor and studying the effect of the device characteristics on various parameters of digital bit streams. It has been found that while the device can be predicted to be suitable for a wide range analog bandwidth application however digital application can be satisfactory only in a narrower range only and that a correlation has been established between digital bit rate and various small signal parameters of the device..

Keywords: pHEMT, Gallium Arsenide, Characterization, Digital Signal Integrity, Eye Diagram

Introduction

High-speed electronic devices form an essential component in microwave communications with ever increasing data rate applications like wireless as well as defence radar and satellite communications. This study aims to examine the behaviour of GaAs devices, which have been a forefront technology for 4G and upcoming 5G for high-speed data rates (Luo et. al, 2020; Zhao et. al, 2018). Most of the work has been around its analogue RF performance characterization however this work involves characterization of the device as well as studies its effects on digital bit rate applications using an eye diagram.

Devices and methods

A high electron mobility transistor is a type of heterogeneous FET (Field Effect Transistor) consisting of several layers of compound semiconductors like a structure made of transitions between GaAlAs, GaAs and GaInAs etc. instead of a traditional single semiconductor. Due to this construction, the electron mobility is nearly double in these devices compared to a standard MESFET and the frequency of operation is thus more than 100 GHz (Zhao et. al, 2018). Fig1(a)

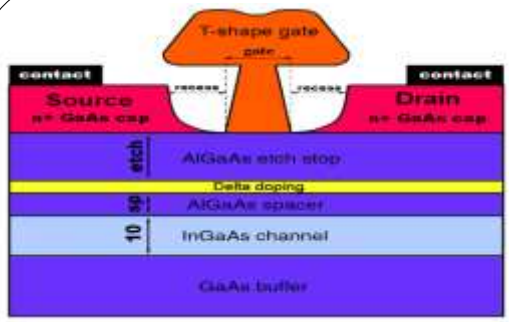


Fig. 1(a): The cross-section of a simulatedp

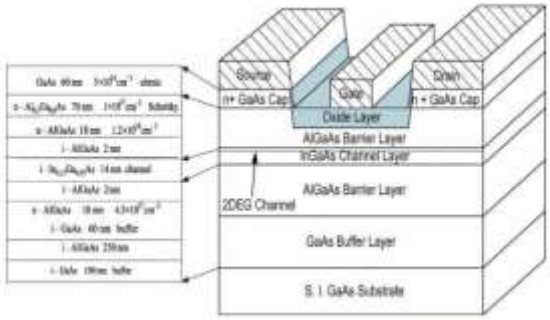


Fig. 1 (b): Cross Section and Physical Dimensions of various layers of a GaAs pHEMTs grown on a GaAs Substrate.

(Source: Kalna et. al 2001)

(Source: Lee et. al. 2005)

Pseudomorphic high electron mobility transistor is one of the HEMT technologies in which the device channel is formed from the InGaAs with 20 -30 % of Indium concentration resulting in a lattice constant mismatch between the channel and the substrate. It is kept so thin that the strain can be accommodated in the crystal with negligible defects. As a consequence, a strained channel is formed in the device. However, the lattice constant of the channel is supposed to be matched with the rest of the device although not fully true, thus is a pseudomorphic channel. With such a structure, the electron mobility of such devices is many folds higher than other devices of the same family (Robertson & Lucyszyn, 2001). Fig. 1(b)

Methods

Below steps have been followed in this experiment. A 0.5x200µm dimension pseudomorphic heterojunction transistor is used to measure the s- parameters using a probe station, modelled through IC- CAP software in the ADS and small-signal parameters extracted and validated. This is followed by an eye diagram simulation and detailed study of the same.

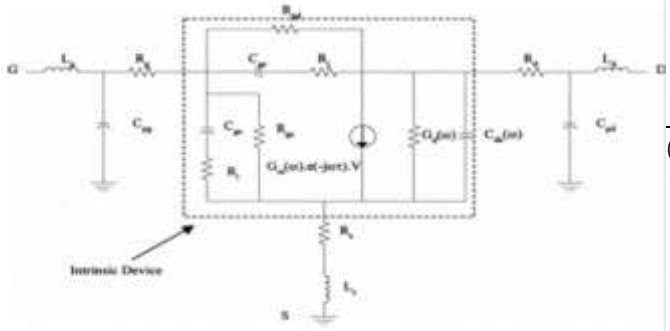
i)S- parameter measurements: In this experiment, the S parameters have been measured directly from the device using a probe station and a vector network analyzer after a 12 step calibration process. S- Parameters are the ratios of

various root square power waves measured under the condition of matched load rather than short and open circuits employed for Z or Y- parameter characterization. Such s - parameter characterization has very less chance of device instabilities and is beneficial regards various other practical considerations.

ii)S-parameter simulations, current gains and other parameters: The measurement files from the network analyzer can be used in the ADS directly or converted to an S2P formatted file to suit for loading into a two-port device in the ADS. The S - parameters can be simulated for any of the two mentioned file formats using an S-parameter simulator from the simulation palette with both the ends terminated into matched load impedances. The currents gains can then be computed from these s - parameters using standard equations. (Hemaizia et. al. 2010)

iii)ICCAP Small Signal Extractions: The above measurement files can also be used to extract the small-signal parameters of the device by the hot and cold method using a standard extraction procedure based on [Broadband Determination MANFRED BERROTH AND ROLAND BOSCH] which starts with de-embedding the internal device from parasitic pad capacitances surrounding it and then the intrinsic device parameters deduced using various subroutines in the ICCAP software to implement the corresponding standard equations. (Sotoodeh et. al. 2000; Selli 2004; Berroth & Bosch 1990).

iv)Small Signal Modeling: The above extracted small-signal parameters can be used to build up a circuit to model the pHEMTs device as shown in Figure 2 below. The s - parameters and the current gains of this circuit can be simulated to compare the previously done simulations for the measurement data itself to compare the model and the actual device for validation.



$$1.\ C_{gs} = \frac{Im(Y11) - \omega C_{gd}}{\omega}\left(1 + \frac{(Re(Y11)^2}{\left(Im(Y11) - \omega C_{gd}\right)^2}\right)$$

$$2.\ R_i = \frac{Re(Y11)}{\left(Im(Y11) - \omega C_{gd}\right)^2 - \left(Re(Y11)\right)^2}$$

$$3.\ g_m = \frac{}{\left(Im(Y21) + \omega^2 C_{gd}\right)^2\left(1 + \omega^2 C_{gs}^2 Ri^2\right))}$$

$$4.\ C_{ds} = \frac{Im(Y22) - \omega C_{gd}}{\omega}\backslash$$

$$5.\ G_{ds} = Re(Y22)$$

$$6.\ C_{gd} = -\frac{Im(Y12)}{\omega}$$

Figure. 2: Small signal model of pHEMT and governing equations
(Source: Kalna et. al. 2001)

The various parameters in the above equations and figure are:

1. C_{gs} is the gate-source capacitance due to charge in the depletion region at the gate-source region the device, C_{gd} the gate-drain capacitance due to

depletion region at the gate-drain space charge layer and is controlled by the gate-drain voltage V_{gd},

2. R_i represents the input resistance of the device. (Hemaizia et. al. 2010)

3. $g_m V_{gs}$ the controlled current source denoting gain of the device- g_m being its trans-conductance and V_{gs} the voltage drop across gate capacitance. R_{ds} is the output resistance of the device, C_{ds} is the capacitance due to coupling of drain and source.

4. The elements R_s, R_d, R_g represent the external resistive parasitics of the device and each constitutes of two resistive components- the contact resistance and the bulk resistance. L_g and L_s represent drain gate and source inductances and are a result of feed pads of the electrodes and finally, the C_{pg} and C_{pd} are capacitance due to electric fields between metallic contacts.

v)Eye Diagram Generation: An eye diagram is a visual display of superposition of consecutive digital bits onto one another and may consist of millions of such bits superimposed on one another to give better information of signal parameters like timing, noise, voltage levels etc. An eye diagram can characterize any digital system in terms of signal quality. "Each eye parameter relates to the health of the transmitted signal and can give a great deal of information, which can be related to the physics of the devices and helps in their optimization" (Venkatesha et. Al. 2005). An eye diagram is usually used at the transmitter side of a communication system in contrast to a BER test which is used at the receiver as communication systems are ultimately judged on their ability to pass bits faithfully without errors (Foster 2004). Analysis of this visual display could give a first-order approximation of parameters like signal-to-noise, clock timing jitter and skew (Breed 2005).

Results and discussions

S – Parameter Measurement and Simulations

Figure 3(a,b,c,d) shows the modelled and measured S parameters of this particular device. For S11 and S12, the trend is seen to comply up to about 23 GHz and deviates a bit afterwards, this deviation being most likely due to manual computation of resistive components of the small-signal model in the IC-CAP. The meaning of this plot is that the reflection coefficient is constant in the range of 0 – 30 GHz (for the measured data plot) above which its value falls below 3 dB point.

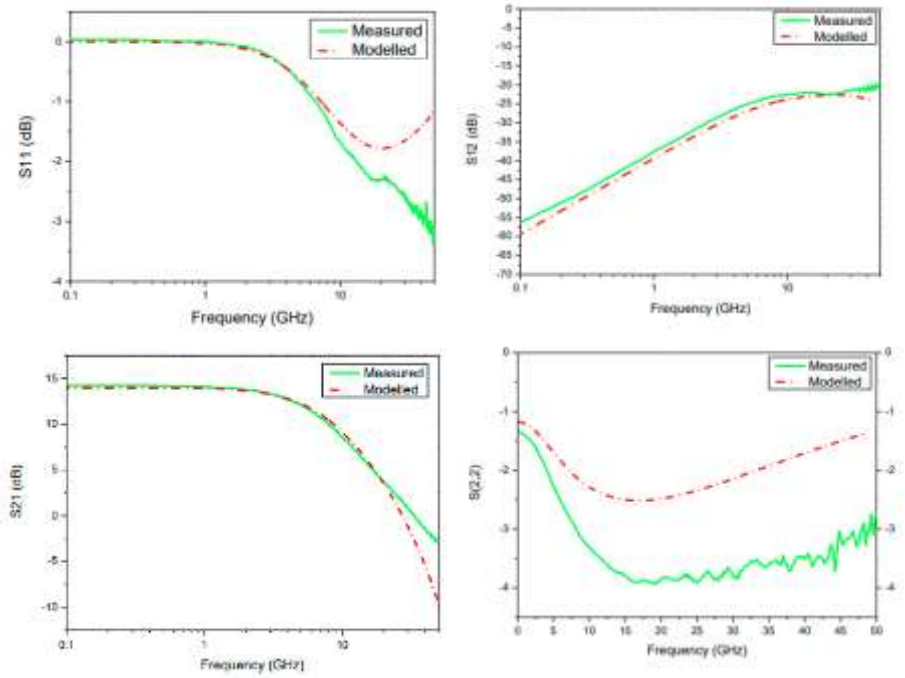


Figure. 3(a,b,c,d) Measured vs Modelled S parameters S11, S12, S21, S22

For S12 the device well follows the measured result. This seems to be more accurate compared to S11 because no manual readings are needed for this parameter thus preventing any errors being introduced. This means the reverse voltage gain increases with increasing frequency and this unwanted reverse gain is due to reverse coupling from output to input ports of the device with increasing frequencies. As we shall see afterwards it is the drain-source capacitance which is responsible for this generally unwanted reverse power flow in the pHEMTs.

Similarly, the modelled S21 parameter also well follows the measured curve but until 20 GHz but doesn't deviate much after this. This plot indicates the device gain falls off with increasing frequencies and as we shall see later how this reduced gain affects the eye diagram for digital input bit streams. This graph represents the forward power flow in the pHEMT and indicates that the gain of the device is constant in the range of 1 -7 GHz after which it starts to fall off linearly. This could be due to recombination of charge carriers at higher frequencies (Venkatesha et. al. 2007).

Finally, the S22 parameter of this device follows the same trend as that of measured response but similar to S11 shows some deviation after a certain frequency range, again due to manual computation of resistive components of the small-signal model in the IC-CAP. This plot shows a decrease in output reflection coefficient with increasing frequencies. Please note that the deviation is likely to be due to errors in vector analyser calibration procedures even with a rigorous twelve step calibration procedure however this doesn't impact the overall trend of the device behaviour for purpose of our study of device behaviour.

Maximum Available Gain and Current Gain

Figure 4(a,b) shows a plot of modelled and extracted current gain and maximum available gain pHEMT device respectively. It can be seen that the gain of the device decreases linearly with increase in frequency and this trend could be attributed again to the recombination of charge carriers at higher frequencies and

other device capacitances (Venkatesha et. al. 2007). The threshold frequency f_t defined as the frequency at which the common gate short circuit current gain fall to unity is found to be = 23 GHz. The maximum frequency of operation which is defined as the frequency at which the maximum available gain falls to unity, f_maxis found to be = 70 GHz and has been found by drawing a line of slope = 20 dB/octave from the point final point of the existing graph until it touches the x-axis

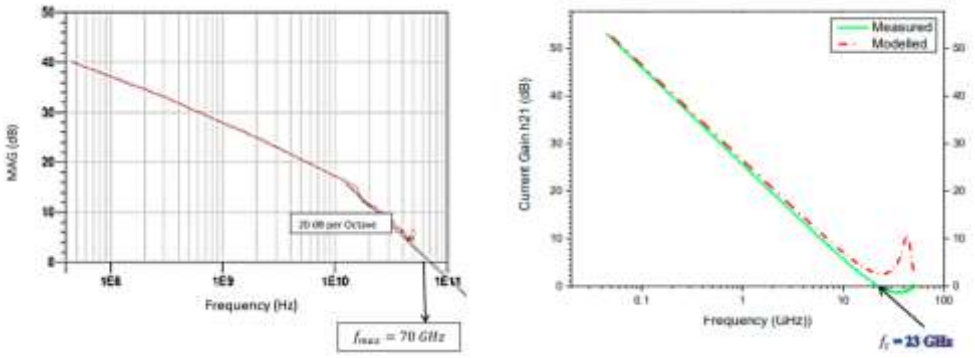


Figure 4(a), (b): Measured vs Modeled Maximum Available Gain and Current Gain

Small Signal Extracted values and Device Modelling in ADS

Table 1 shows the extracted small-signal parameters of the circuit shown in Figure 5 below It can be seen that the extracted values in Table1 very well fit in the expected range of a typical pHEMTs device but deviate quite largely for some of the parameters like C_gs, L_g, L_s and could be due to different approaches of handling the ICCAP modelling software (e.g., choosing different points while interpolation). However, to check for accuracy of extracted values, eye diagrams were generated both measured and compared small-signal parameters and were found to be almost the same except for some minor eye parameter differences. Furthermore, the measured results were also compared with other published work (Tayel 2009) and were found to be within normal range except for a small deviation in a few parameters which again can be attributed to different approaches to the extraction procedure itself.

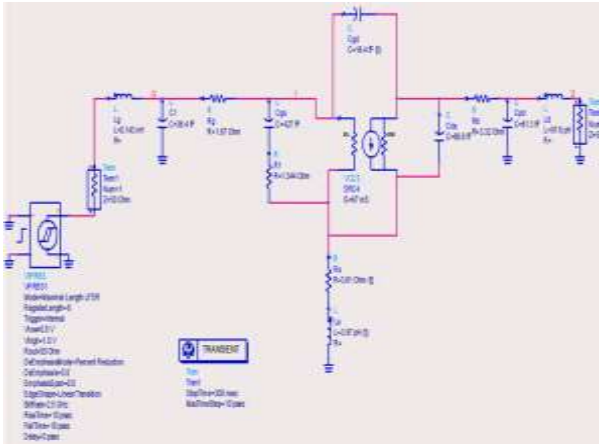


Figure 5: Schematic of Simulated Circuit in ADS

Parameter	Name	Description/ Dependence of the parameters to the device physical structure	Extracted Values	Extracted values from other works[5,6,7]
Cgs(fF)	Gate source capacitance	Interaction of the channel charge and the gate metal	427	184
Cpg(fF)	Gate external lead capacitance	Parasitics of external pad connections on gate side	36.4	43.26
Rg(Ω)	Gate resistance	External lead resistance	1.673	2.404
Ld(pH)	Drain inductance	External Lead Inductance	97.6	27
Cpd(fF)	External lead capacitance	Parasitics of external pad connections on drain side	61.3	26.53
Rd(Ω)	External drain resistance	Self-heating and the temperature dependence of the parasitic resistances	3.32	2.311
Ro(Ω)	Output drain resistance	Self-heating and the temperature dependence of the parasitic resistances	1.67	1.67
Lg(pH)	Gate inductance	External Gate lead Inductance	143	26.58
Cgd(fF)	Gate Drain Capacitance	gate and drain metal periphery and the coupling of the gate metal with the semiconductor caps	16.4	67
Cds(fF)	Drain Source Capacitance	buffer and channel layers depending on the channel carrier distribution	66.6	54.09
Gds(mS)	Output conductance	Self-heating and the temperature dependence of the parasitic resistances, especially the gate resistance	1.68	5.4
Ls(pH)	Source Inductance	External parasitic Inductance	3.97	129.2
g_m (mS)	Transconductance	Gate Width	67	46

Table 1: Extracted values and comparisons

The extracted small-signal parameters can now be used to develop a small signal equivalent circuit in the ADS and simulated again for the S- parameters, maximum available gain and current gains. These results can be compared with the previously generated s- parameters and can be studied for any deviation between the measured and the modelled results.

Eye Diagram Generation

Below method can be used to generate an eye diagram in the ADS:

ADS Front Panel Eye Method: This being the standard method of generating eye diagrams has been used and gives all the measurement data of the eye diagram with convenience. It starts by defining the desired trace and inclusion of bit rate expression in the ADS Front Panel.

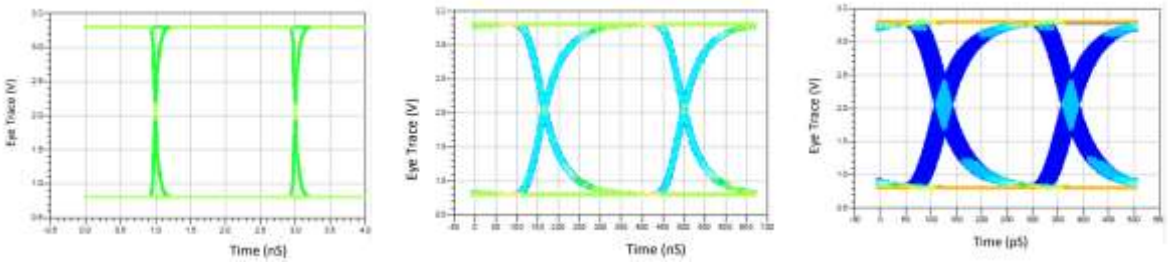
To generate an eye diagram in the ADS front panel, a schematic as shown in Figure5 above was created in the ADS schematic window and an 8-bit pseudorandom bit sequence was used, although other sequences were also tested during simulations. A higher number of bits could be used to generate extra frequency contents for high analysing device behaviour minutely.

Eye Diagram Analysis and Discussion

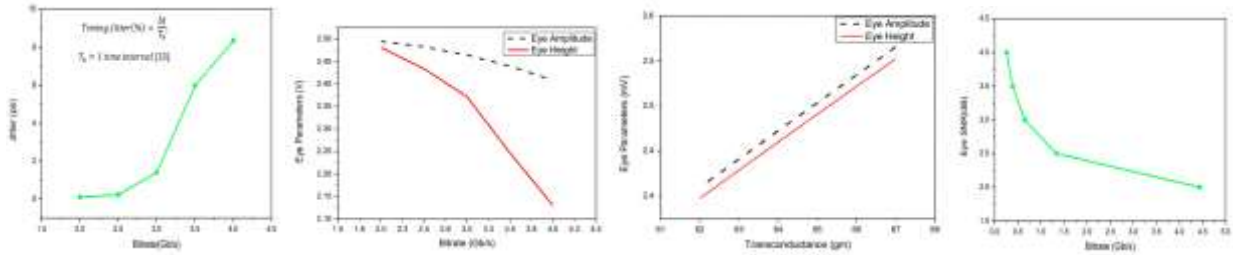
Figure 6(a) shows an eye diagram for a 0.5 GHz digital input to the pHEMT device and it can be seen that there are very less timing errors and it is wide open clearly and logic decision making would be easier at the receiver. Similarly, it can be seen from Figure 6(b) that the digital signal has degraded a bit on increasing the input data rate worsening the eye at above 4 GHz. Thus although the pHEMT may give a significant gain well up to 25 GHz, as predicted from s parameters but for digital applications, the received signals would be almost impossible to recover at the same frequency. The same eye diagram can now also be used to plot other valuable information about the device giving a very good insight of what to expect the response of the device to the digital input signals in terms of timing, SNR, eye rise and fall times etc.

It can be seen from Figure 7 that both the eye height and eye amplitude decreases with increasing bit rate with input bitrate having very much pronounced effect on eye amplitude than eye height. The eye amplitude can be seen to decrease exponentially after about 3 GHz input. As we know that the eye height is lower than the eye amplitude due to noise, and the eye amplitude may

decrease due to signal attenuation, it could be concluded that the noise in the system increases exponentially resulting in reduced eye height. The attenuation doesn't seem to decrease too far with increasing bit rate compared to eye height.



Figures 6(a,b,c) Effect of various bitrates on Eye diagram



Figures 7(a,b,c,d): Effect of different bitrates on Jitter, Eye Height, Eye Amplitude, Eye SNR

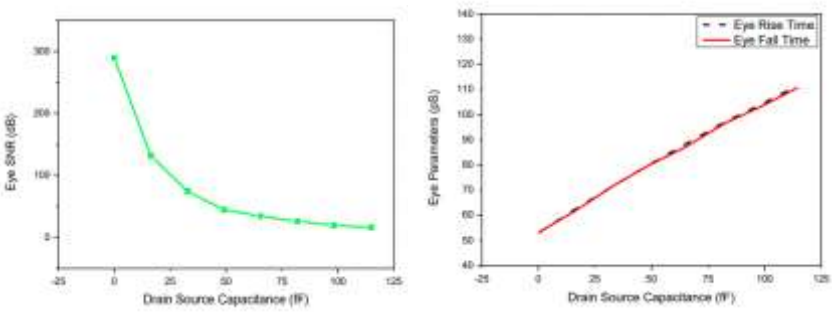
It can be seen from above Figure 7(a) that the Jitter increases with increase in input bitrate and the steep is very much pronounced after 3 Gbps bitrate makes the system prone to errors beyond this bitrate. One of a few techniques that could be used to decrease this jitter would be to suitably use a CPW as an inductor and an active source follower along with the pHEMTs to broaden its bandwidth to compensate for the boding lead capacitances (Ding et.al. 2005).

It can be seen from Figure 7(b, c) that the eye amplitude and eye height increase linearly with an increasing transconductance of the device, this being so because the gain of the device being dependant on gm, results in a large signal output, quite distinguishable from noise levels.

It can be seen from the Figure 8(b) that the eye rise and fall times increase linearly with the drain-source capacitance which means the digital bit stream has been corrupted and could result in bit errors at the receiver with increased capacitance. This should be taken into consideration while designing the device for a particular bit rate application

Transconductance(mS)	67	66	65	64	63	62
Eye Level Zero(V)	0.81292	0.837252	0.86164	0.88616	0.91082	0.93554
Eye Level One(V)	3.33848	3.321854	3.3153	3.3087	3.30207	3.29546
Eye Level Mean(V)	2.0737	2.079553	2.08847	2.09743	2.10644	2.1155
Eye Amplitude(V)	2.51556	2.484682	2.45366	2.42254	2.39125	2.35992
Eye Height(V)	2.50239	2.471788	2.44088	2.41002	2.37889	2.34759
Eye Height (db)	3.98355	3.930077	3.87564	3.82021	3.76375	3.70621
Eye Width(V)	4.90E-10	4.75E-10	4.77E-10	4.82E-10	4.86E-10	4.93E-10
Eye Opening Factor	0.99758	0.997585	0.9974	0.99742	0.99745	0.9976
Eye Signal_to_Noise	413.969	379.4476	384.71	387.12	391.598	417.117
Eye Duty Cycle Dist	1.21E-13	3.73E-12	2.74E-12	2.61E-12	1.70E-12	9.40E-13
Eye Duty Cycle Dist(%)	0.24276	0.746136	0.54715	0.52171	0.34011	1.88E-01
Eye Rise Time(s)	6.24E-11	6.21E-11	6.26E-11	6.26E-11	6.27E-11	6.30E-11
Eye Fall Time(s)	6.24E-11	6.27E-11	6.28E-11	6.25E-11	6.27E-11	6.33E-11
Eye Jitter (PP)	1.11E-11	2.65E-11	2.24E-11	1.70E-11	1.34E-11	8.96E-12
Eye Jitter (RMS)	2.79E-12	7.68E-12	6.24E-12	5.41E-12	3.96E-12	2.26E-12

Table 2: Measured Eye parameters



Figures: 8(a)(b): Effect of drain-source capacitance on the eye diagram

Table 2 below shows various eye parameters that can be seen to vary with input data rates. Since the noise, distortion, timing errors, and rise/fall times are of utmost importance in any communication system, these were thoroughly analysed and are as follows:

We can see from Figure 8(a) that SNR reduces significantly with increasing bitrate though not a large steep after 1.5 Gbps. This could be due to heating, impact ionization, and trapping which contribute to transient behaviour through rate-dependence mechanism (Ketkar et. al. 1999; Parker & Rathmell 2003).

It can be seen from Figure 8(b) that with an increase in the drain-source capacitance the SNR decreases exponentially making it very prone to errors at higher capacitance values. It can be seen that this capacitance has a pronounced effect on eye SNR as should be because it is well known, that this capacitance is the component of the model responsible for reverse power flow in the circuit. More this capacitance, more the reverse coupling between output and input resulting in oscillations along the path and should result in losses and noise. Since losses could not have been a prime concern for such small devices, quality degradation due to lowering of SNR cannot be overlooked. Increasing it continuously leads to the closure of the eye, the effect being more pronounced than on increasing the bit rate.

Conclusions

In this project, the measured s - parameters of a pHEMTs device have been used its extract small-signal parameters and this model has been used to generate an eye diagram for different bit rates and small-signal parameters. It has been seen that although a device may be characterised to be using for a wide range of signals using the s - parameters, however for the digital applications the input bit rates that could be used by the device at its input is quite narrow. We have compared the effect of varying input bit rates on eye amplitude and the eye height of the eye diagram and it has been seen that eye height is affected comparable lesser than the eye amplitude and indicates that the device can be used very well in the range where the eye amplitude has fallen significantly because the eye height takes into account the noise errors. We have also seen how the eye amplitude and eye height behave with transconductance, gm of the device. The gain of the device being dependant on this transconductance affects the quality of the digital signals linearly. The jitter and the dependence of Eye SNR have also been investigated for variable input bitrates and are reported to show an exponential trend meaning the timing errors are much more likely to dominate rather than the attenuation of the signals through the device. Some form of methodology needs to be implemented to keep away from timing errors especially for higher data rates rather than doing away with signal attenuation because the signal attenuation can be compensated by amplifying action or in other words by increasing the gain of the device. Finally, the effect of drain-source capacitance on the Eye SNR and rise/fall times have been investigated and it has been seen that while as the eye rise/fall times increase linearly with increasing drain-source capacitance, the eye SNR worsens exponentially with increasing drain-source capacitance. Thus the two parameters discussed above – the bitrate and the drain-source capacitance, are reported to have a pronounced effect but on different parameters of the eye diagram. The bitrate affects the eye in a more pronounced fashion in terms of jitter while as the drain-source

capacitance reduced the eye SNR exponentially. This, in essence, means that if we can somehow decrease the drain-source capacitance, the system could be improved significantly, instead of increasing the gain of the device which is not reported to have such large effect on the timing of the eye diagram.

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